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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,820	05/14/2001	Ruben Madrid	018865007400	9693

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EXAMINER

WOJCIECHOWICZ, EDWARD JOSEPH

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/855,820

Applicant(s)

Madrid

Examiner

Edward Wojciechowicz

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-28 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) All b) Some* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) Notice of References Cited (PTO-892) 18) Interview Summary (PTO-413) Paper No(s). _____
- 16) Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) Notice of Informal Patent Application (PTO-152)
- 17) Information Disclosure Statement(s) (PTO-1449) Paper No(s). 4 20) Other: _____

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9, 10, 12, 13, 17, 18, 19, and 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda et al. Takeda shows the basic structure and process of the claimed invention with a carrier for a semiconductor die which comprises a metal layer and a plurality of bumps formed in the metal layer, and wherein the carrier electrically couples the semiconductor die to a circuit substrate. See, for example, Fig. 7 of Takeda, where a metal carrier member (8) has a plurality of stamped bumps formed therein, i.e. the raised end portions which contact the solder bumps (3) on the semiconductor die. As can also be seen in Fig. 8 of Takeda, additional bumps (13) are formed on the opposite side of the carrier so as to electrically couple the die to a circuit substrate, as claimed. The carrier member of Takeda also includes a dielectric layer on the metal layer. In addition, Takeda also teaches the claimed method steps of claims 24-28.

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3.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 8, 11, 14-16, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda, and further in view of applicant's admitted prior art as discussed in page 1 of the specification, as related to prior art Fig. 1, and Akram. While the Takeda reference teaches the main structural and process features of the claimed invention, Takeda does not specifically refer to vertical MOSFETs formed in the semiconductor die, nor to the specific shape of the raised bump contacts. However, as stated in the description of the prior art on page 1 of the specification, incorporating such vertical MOSFETs in a die bonded semiconductor device as claimed, is well known in the art. See, specifically, the recitation at lines 25-30 on page 1 of the specification. Clearly, the motivation for including such MOSFET devices to the Takeda semiconductor die would be the obvious fact that MOSFET devices are routinely included in semiconductor integrated circuits as described by Takeda.

Likewise, while Takeda does not specifically discuss the dimensions of the carrier bumps in his device, Akram shows a similar device using a bump mounted carrier plate to attach a semiconductor die, where the bumps have a thickness equal to or greater than the thickness of the semiconductor die. See, for example, the structure shown in Fig. 4 of Akram, along with the

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discussion at col. 6, l. 31-47. The shape of the bumps employed in Akram would also appear to meet the claimed limitations with a conical shape. This structure serves to protect the die from unwanted stresses, and the motivation to employ this structure in the device of Takeda would be to also protect the die.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to E. Wojciechowicz whose telephone number is (703) 308-4898, or to SPE Eddie Lee, whose number is 703-308-1690.



EDWARD WOJCIECHOWICZ
PRIMARY EXAMINER

EW:ew

March 10, 2002